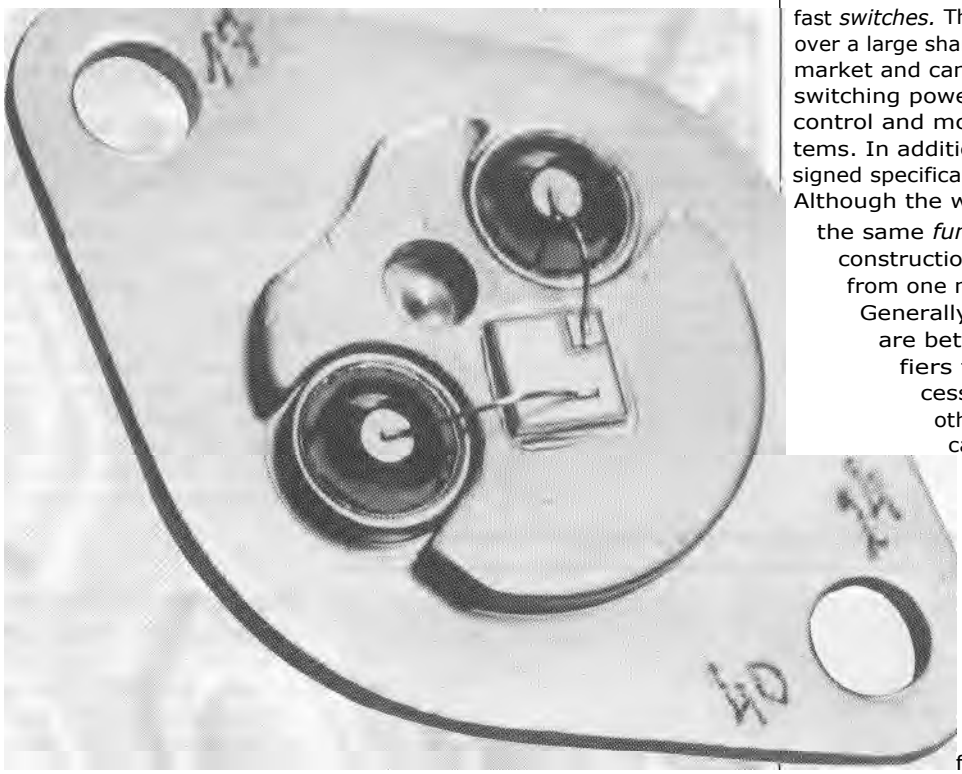
introducing DMOS power FETs



New power FETs seem to be christened almost every day: VFETs, HEXFETs, DMOS, TMOS and SIPMOS, to mention but a few. Despite their different names, they all have a great deal in common, as far as their characteristics, structure and applications are concerned. This article takes a look at power FETs in general, paying special attention to the fast-switching DMOS branch of the family.

The term VFET will sound familiar to most readers, although few are likely to have actually seen one 'in the flesh'. Not that they are much to look at, but it does go to show that VFETs have as yet failed to attract the amount of popularity they deserve. Way back in 1976 (see the Elektor April issue of that year) VFETs were billed to be the (almost) ideal output transistors for (audio) amplifiers. Due to their high price and poor availability, however, they never quite made it into the limelight. But then, this is just one of those vicious circles, for components don't drop in price and become easy to obtain until they are already popular .. .

About a year ago, a new branch was welcomed to the VFET family: the DMOS series. Basically, they are very similar in operation to VFETs, but their structure is slightly different and their switching times are much faster. DMOS FETs are in fact mainly promoted as fast *switches.* They are predicted to take over a large share of the power transistor market and can be used in converters, switching power supplies and in relay control and motor speed control systems. In addition, some types are designed specifically for RF purposes.

Although the whole DMOS family has the same *fundamental* structure, the construction of the gate may vary from one manufacture to another. Generally speaking, VMOS FETs are better suited as RF amplifiers than their DMOS successors. The latter, on the other hand, are more vertical in structure (as will be seen later on) and are therefore capable of handling higher voltage levels.

Before we go any further, let's take a look at the main characteristics of the VFET family as a whole and disregard their individual traits for the moment. First of all, we need to find out how FETs differ from their well-known bipolar counterparts. (Anyone with a special interest in this field might like to read the data books referred to at the end of this article.) To put it in a nutshell, FETs cost less than bipolar types, switch faster (in a few nanoseconds), afford higher input impedances with low drive parameters and have widely extended the range of circuit possibilities.

At the time of going to press, the new DMOS transistors were still very difficult to get hold of in the retail trade and those that were to be had were far from cheap. Nevertheless, we have every reason to believe that this situation will change within the not too distant future.

all that often, so it might be a good idea to recap on some of their features. Normally, MOSF ETs have a high input impedance and a fairly average mediocre gain. They are suitable for use at high frequencies (up into the gigahertz range), but can only handle low power. Consequently, they are mainly used in receivers. Their basic operation is shown in the form of a block diagram in figure 1.

The source and the drain are both bonded with an n zone within a p substrate. Thus, as in ordinary transistors, a npn structure is involved. This may be represented as two diodes connected back-to-back, as a result of which no current is allowed to flow from drain to source.

When the gate is made positive, electrons collect in the p material bordering the gate (electrons are negatively charged particles and are drawn by the positive gate). The p material around the gate now contains an excess number of electrons and has therefore become an n region. A channel is thus formed between source and drain consisting entirely of n doped material. Furthermore, since conduction can take place, current can now flow. The higher the voltage across the gate, the wider the channel and the lower the resistance between source and drain.

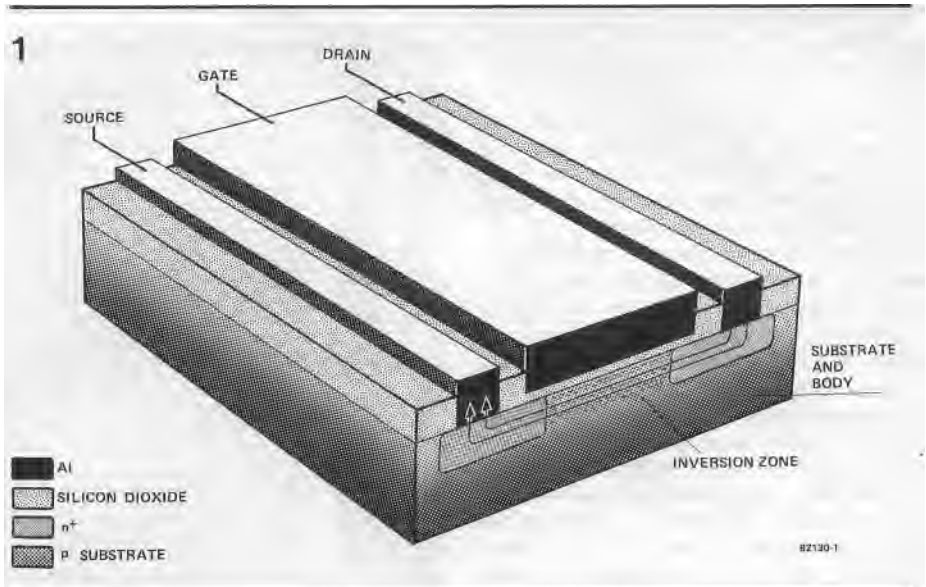
Figure 2 shows a VFET in cross-section. Again, a p region separates the source and drain, both of which are bonded with n regions.

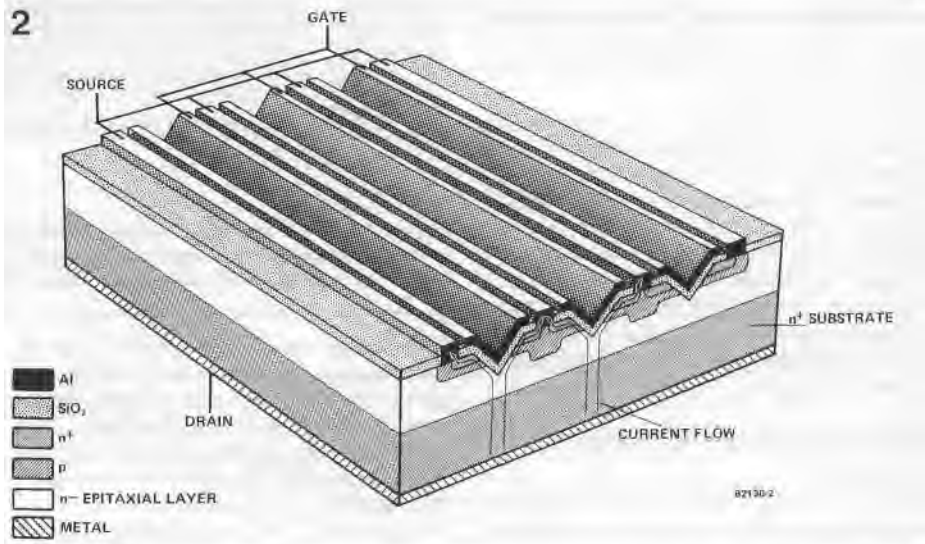
The principle is the same as in figure 1: when the gate is made positive, a conductive channel is formed in the p region, allowing a current to flow between drain and source.

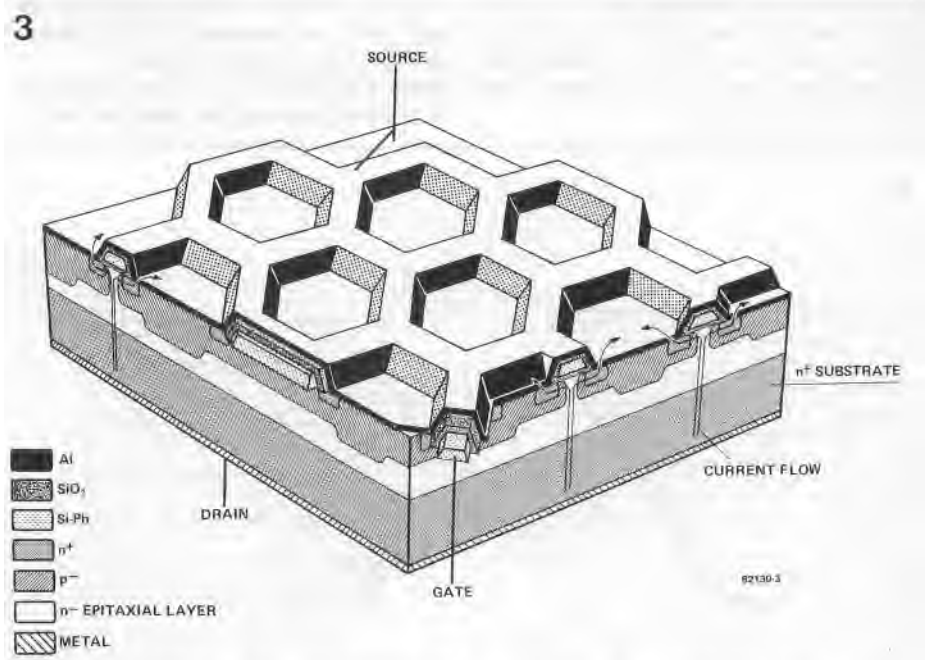
That covers the basic operation of a VFET. The 'V', by the way, stands for vertical (the direction in which the current passes through the substrate) and has nothing to do with the V-shaped groove in the substrate.

The reason why a VFET can handle high power better than an ordinary FET is purely due to its format and not to any great technological achievement. The cost of semiconductors is largely determined by the size of the chip. An ordinary, planar power FET would have to be relatively large in order to cope with the same amount of power. The area occupied by the drain connection has been economised on in the VFET and the drain is now situated underneath the chip. Furthermore, the channels are formed by means of diffusion, enabling the VFET to operate at much lower tolerance levels. The result is a much smaller chip incorporating a few thousand FETs in parallel, (as can be seen in Photo 1). Thus, it is not a question of a single VFET being able to take on an army of amps, but a whole host of them hold the fort!

DMOS FETs will seem quite straightforward in comparison. Here the gate is completely surrounded by an insulating layer of silicon dioxide (SiO_2) and the







Figures 1, 2 and 3. Block diagrams showing an 'ordinary' FET, a VMOS FET and a DMOS FET, respectively. While the FET is not conducting it functions as a cutoff diode. When it *conducts* the diode effect gradually disappears until only a slight on-resistance is left, (when the transistor is fully driven).

hexagonal (HEXFETs, etc) are also possible, according to the preferences of each particular manufacturer.

So much for the structure of DFETs. It should be noted that some types specifically designed for audio or RF applications do not follow this rule.

The DMOS structure just described has a disadvantage in that the gate combines a certain amount of internal resistance with a rather large capacitance (several nano-farads). When driven with a signal in the MHz range, the gate may well get so hot under the collar that the whole FET will go up in smoke! This is where VFETs are at an advantage, for their gate can be made of aluminium, which considerably reduces the internal resistance. This is also the reason why DFETs are advertised as *switches* rather than RF components.

But what you lose on the roundabout, you gain on the swings, and DFETs are able to deal with relatively high voltages. Great field intensity is produced at the bottom of the V shaped groove in VFETs and the various etching and diffusion processes down there are very difficult to control. Fortunately, these snags do not exist in planar DMOS FETs and the latter also have a higher breakdown threshold.

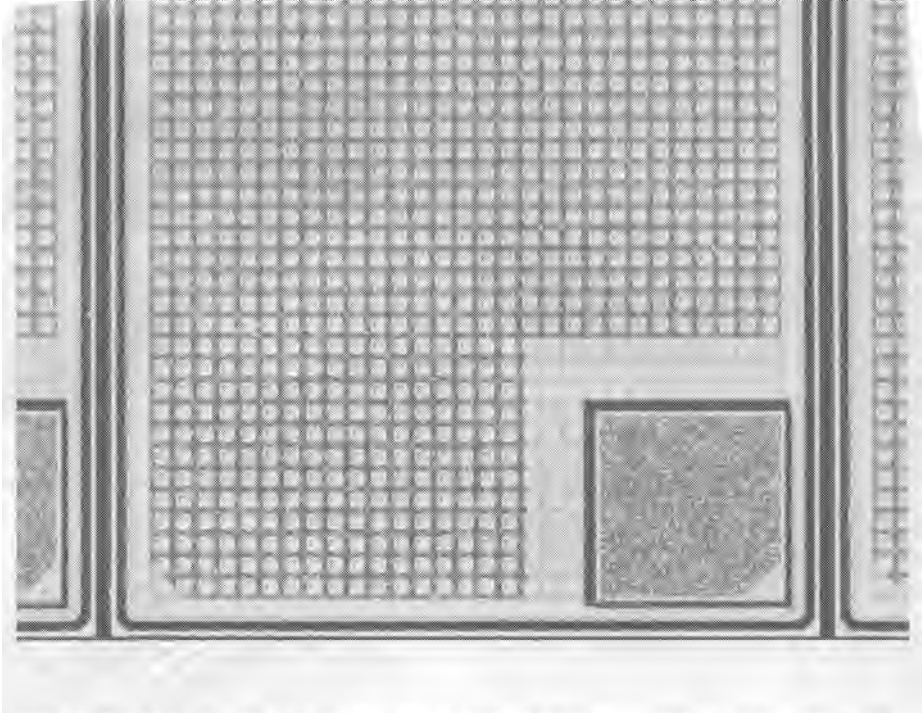


Photo 1. A DFET consists of a large number of FETs that are connected in parallel. The square in the top lefthand corner represents the gate, whereas the rest of the upper surface is taken up by the source (the whole top surface is plated through).

DFETS: do they come up to scratch?

For one thing, DFETs dissipate about the same amount of power as a transistor in a similar package. Then there are types that can withstand up to 1000 V and others that can switch up to 25 A. As in bipolar transistors, the maximum current level may even be higher than that — for *brief* periods!

Constructors are recommended to go by the $R_{ds(on)}$ (= maximum on-resistance) rather than rely on the current ratings provided by the manufacturer. The lower the $R_{ds(on)}$ the more current the FET can handle. Be sure not to exceed the maximum dissipation rate!

The gain of a FET is expressed in terms of its slope and is a couple of amps per volt, the threshold voltage being one or two volts. An example of the current voltage ratio is given in figure 4.

Since a MOSFET is involved, no power is required to drive the gate, as there is no current flow. Thus, the power gain of DFETs is ideal: it is infinite! Unfortunately, this feature does not have any practical advantages. A fair amount of power is certainly needed during the switching process, as the gate capacitance of several nanofarads has to be transferred. If the capacitance transfer takes too long, in other words, if the gate is fed a slowly changing voltage, the FET will be unable to switch as fast as usual. Although the whole FET family is noted for its remarkably rapid switching capabilities (they switch cur-

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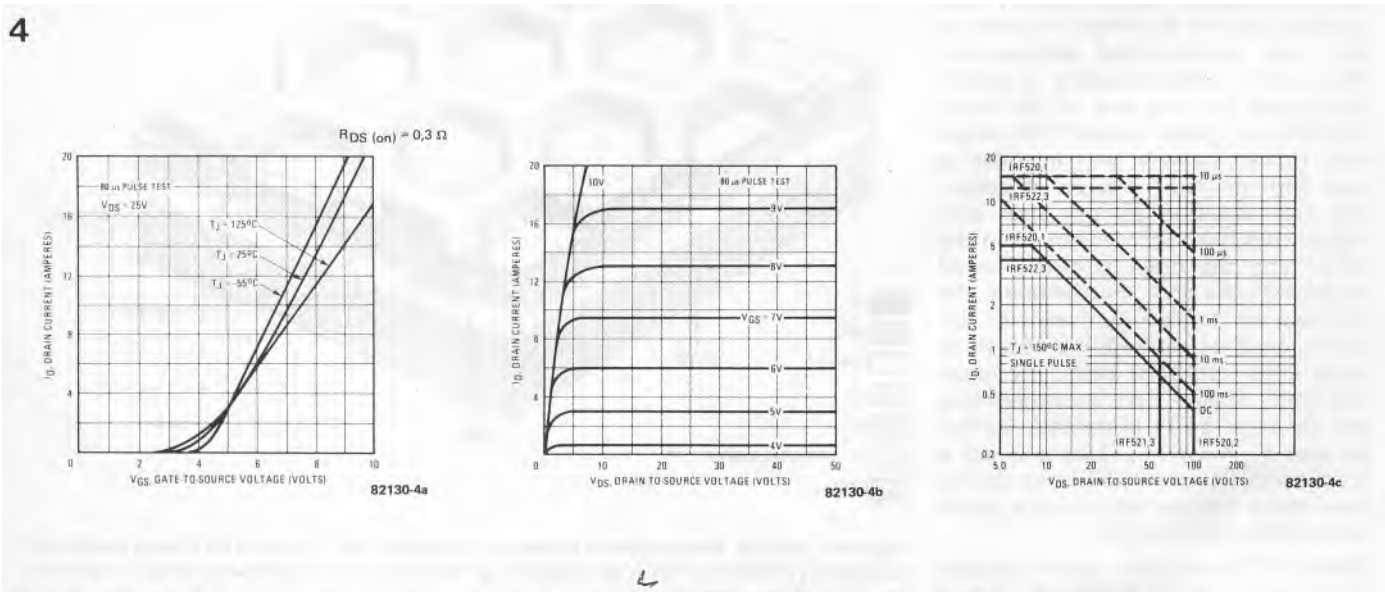

Figure 4. These graphs show the characteristics of a FET. Similar curves apply to other members of the power transistor family.

rent in about twenty nanoseconds), this speed can only be reached provided the gate voltage is a perfect square wave. In practice, the gate voltage looks far from symmetrical, as can be seen from the (slightly exaggerated) example given in the second photograph). The top trace shows a symmetrical square wave driving a CMOS 4049 inverter. The output of the 4049 is connected directly to the gate of a DMOSFET (in this case a BUZ 10). The signal edges leave a lot to be desired and tend to form 'kinks' half-way down the curve. The bottom trace represents current passing through the FET.

Clearly, it takes the CMOS inverter quite a while to alter the gate voltage, for the gate capacitance can only be transferred with a couple of milliamps. As the 4049 is designed as a TTL buffer, it enables more current to flow to ground than to the positive connection. Not surprisingly, the falling edge is much steeper than the rising edge.

But why is the strange kink formed in both edges and why is it more pronounced in the slower, rising edge? Well, the gate/drain capacitance is mainly responsible for this. Figure 5 shows a simplified equivalent circuit diagram which valve lovers will immediately recognise as the 'Miller' effect.

The rising voltage across the gate causes the drain voltage to drop. The signal alteration is passed on to the gate by way of the gate/drain capacitance and, as a result, the gate voltage will only be able to rise very slowly. This situation continues until the drain voltage cannot drop any further. The effect is clearly visible in Photo 1, where the gate voltage is relatively constant while the drain voltage alters. In addition, there is almost always a certain amount of inductance in the source connection and this enhances the effect by making the source slightly negative. At a higher supply voltage, the gate/drain capacitance transfer will obviously take longer.

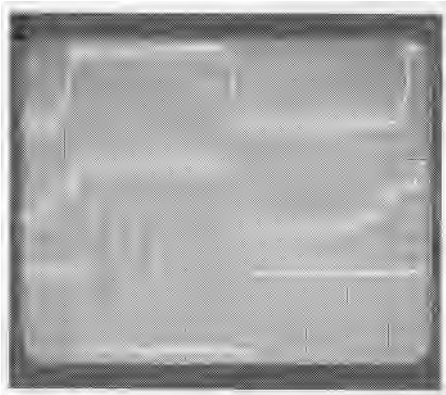

Photo 2. When a power FET is driven from CMOS, considerable delays are caused because the driver cannot produce enough current for a rapid gate capacitive transfer. From top to bottom: The CMOS buffer control, the waveform at the gate of the FET and the current passing through the FET.

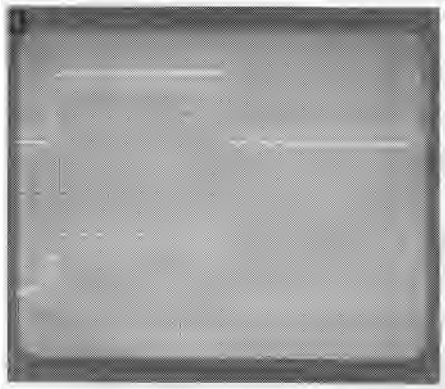

Photo 3. Better switching times are obtained by driving power FETs from a TTL open collector buffer. The gate control voltage can best be selected at twice the level of the drive voltage. This will produce fairly even edges in the drain current. A higher voltage allows the power, required to drive the gate, rise quickly (with the square of the voltage) and does *not* cut down the time.

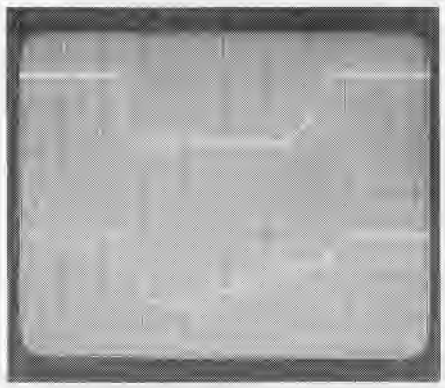

Photo 4. The gate voltage during the switching process. It is very difficult to predict the exact time delay, because the related gate capacitances are dependent on the (intermediate) drain voltage levels. The same thing applies to the driving power requirements, which is why some manufacturers provide graphs showing the gate voltage waveform at different drain voltage levels.

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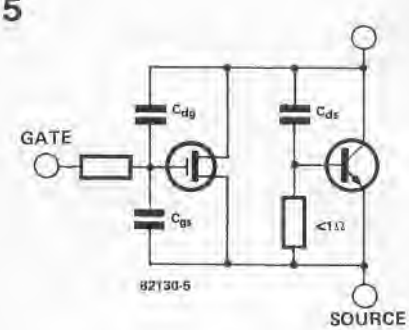


Figure 5. An equivalent, simplified circuit diagram for a DFET. The drain/source capacitance is of particular significance when driving the transistor. A transistor is connected in parallel to the FET and acts as a diode (by way of the 1 Ω resistor and the base/collector junction) in the case of negative drain voltages. The diode can handle the same amount of current as the DFET, although it is of course much slower.

In short, the actual switching time is mainly determined by the circuit driving the gate. The time achieved depends on the drain source voltage (the higher this is, the longer the process takes), on the gate capacitances (which in turn depend on the FET used) and on the driver circuit (regulated by the user).

Photo 3 shows a FET driven from TTL, which is a lot faster. High speed switching does, however, entail one or two difficulties. If a current of a couple of amps is flowing through the FET and is interrupted in a matter of nanoseconds, appallingly little self induction is needed in the drain network to cause a considerable peak voltage ('spikes'). The peak voltage must be added to the supply voltage and should the sum exceed the drain source voltage rating of the FET, the transistor will 'kick the bucket' at once. The solution is to construct the circuit carefully and connect a freewheeling diode to the power supply. Alternatively, a zener diode may be connected in parallel to the FET. It is not really advisable to use an RC network, as a slowly decaying oscillation can rarely be avoided and, in the event of an ill-chosen RC time, it could make matters far worse!

'Spikes' in the drain voltage also affect the gate voltage by way of the drain/gate capacitance. If the gate is driven at a high on-resistance, the maximum gate/source voltage may easily be exceeded — and the constructor will end up having to buy a new FET. Either drive the gate with a low on-resistance and/or connect a zener diode between the gate and source.

Readers will have gathered from the above that this type of power FET does not incorporate an internal protective diode (zener diode). This is not necessary, because of the relatively high gate capacitance, as a result of which 'spikes' can only be caused by an inordinate amount of static charge. The lack of diodes has the advantage that the constructor can drive the gate without any compunction. Negative voltages in particular will no longer present any problems (provided they are not too large). All in all, due care must be taken with regard to static charges when handling DMOSFETs!

Paralleling DFETs

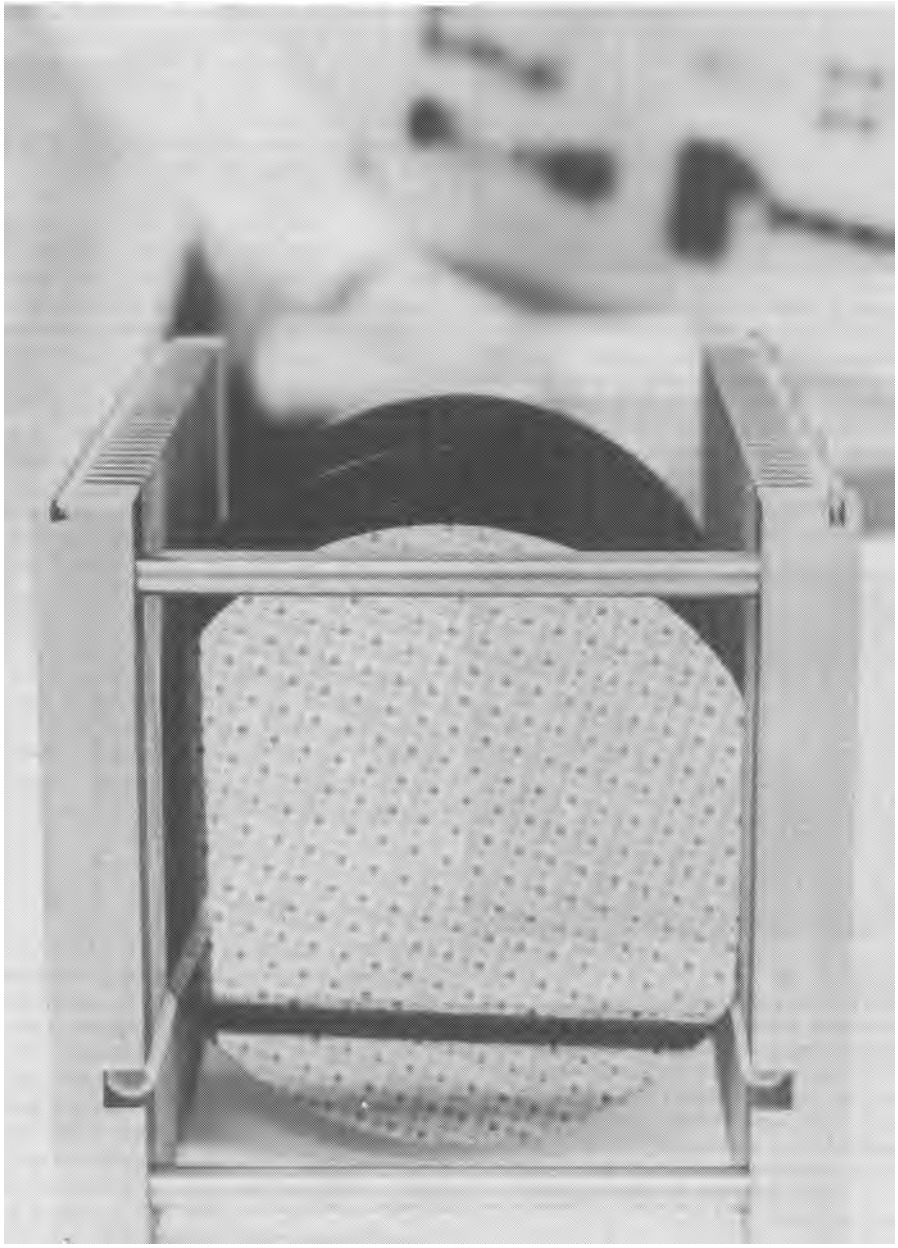
Normally speaking, DFETs can quite easily be connected in parallel, because the semiconductor material provides greater resistance at rising temperatures. The $Rds_{(on)}$ will then increase. This ensures that the hottest transistor will automatically consume less current and therefore dissipate less heat. Figure 4a shows what effect this has on the graph: the *maximum* current is lower at a high temperature. But the opposite is true of current levels below 2A.

So far, so good. Should FETs with mismatched VGS characteristics be connected in parallel, the FET with the minimum gate voltage will be driven 'on' first and will temporarily have to do all the work. A second problem may involve oscillation at extremely high frequencies (above 100 MHz). The constructor should keep this in mind and try to match the VGS levels of the FETs to within about 5% of each other. To be on the safe side, include a couple of low value resistors in each gate connection. Two birds are killed with one stone: the oscillation is suppressed and the drive potential is better distributed.

Cooling

DFETs are available in the same packages as bipolar transistors. They are easy to mount on a heatsink (whether they are insulated or not).

Cooling is absolutely vital where FETs are involved. When we discussed how to connect two DFETs in parallel, we mentioned the fact that the Rds(on) has a positive temperature coefficient and that this was an advantage in that particular instance. Unfortunately, this behaviour certainly does not benefit dissipation, for the hotter the FET and the greater its resistance, the higher the dissipation. The result is a vicious circle: the temperature rises even further! This may lead to regenerative feedback and inevitable death of the expensive DFET. Such detrimental effects are avoided by keeping the temperature as low as possible. By cooling the transistor, the saturation voltage risk is kept to a minimum and any overheating is prevented. The best rule-of-thumb is simply to use a 50% larger heatsink than normal.



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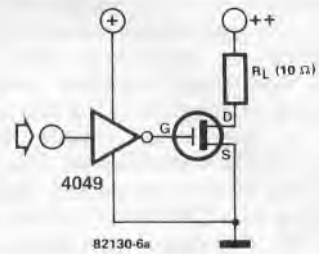

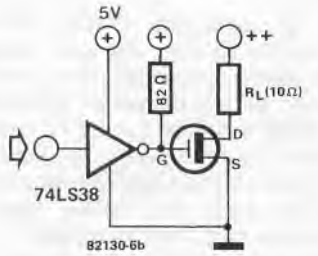

Figure 6. Provided the switching speed parameters are not set too high, DMOS FETs can be driven in a very straightforward manner. In figure 6a the DFET is driven directly from a CMOS gate with a supply voltage of about 10 V. In figure 6b the DFET is driven from TTL with an open collector output. In most cases, the pull-up resistor will have to be fed with a higher voltage than the 5 V TTL supply.

Background literature

The 'HEXFET Data Book' from International Rectifier makes an excellent read.

The Siliconix 'VMOS Power FETs Design Catalogue' also provides plenty of information.

Then there's ITT's book on 'VMOS transistors, their features and applications'.

Other titles include:

'Hitachi Power MOSFETs' by Hitachi and

'SIPMOS Power Transistor' by Siemens.